



Cross Conduction Inhibit

Power supply design using switching logic requires attention to cross conduction problems. Many switching circuits fall short in performance due to lack of attention to this problem. Failure to remedy cross conduction results in premature transistor failure, excessive noise in the output, low efficiency, and excessive heat.

Typically, the method to prevent cross conduction is to provide a 'dead time' (both transistors off) between alternate drive pulses. This dead time is usually of sufficient duration to assure that the 'on' states of the power transistors do not overlap under any conditions. There is variation in the storage time of similar power devices. Also, the storage time of the transistor (time to turn completely off) is a function of temperature, drive circuit, and collector current. Therefore, to insure a safe margin, the typical dead time will be several per cent of the drive time, and this will reduce the efficiency and the range of the pulse width control.

The basic components for a dynamic cross conduction inhibit technique is shown above for use in a push-pull converter. This technique will allow a pulse width control range to extend to 100%, without a risk of a cross conduction problem. Cross conduction will generate large current spikes in the collectors of the transistors and this excessive stress may cause failure of the transistors.

For an initial condition when Q2 is just about to turn on (point t on the waveform). At this instant, input pin 4 of gate U1B is enabled for an 'on' state of Q2. However, as a result of its storage time Q1 will still be conducting and its collector voltage will be low. Hence input pin 5 of U1B will be low. As a result of the gating action of U1B, the turn on of Q2 is delayed until the voltage on the collector of Q1 goes high. This does not occur until the end of the storage time, when Q1 turns completely off. As a result, cross conduction is prevented. Q2 only turns on after Q1 turns fully off. The same action occurs when drive is applied to U1A, except in this case the turn on of Q1 is delayed until Q2 turns off.

This gating action is self-adjusting and will accommodate for variations in the storage time of the transistors. Being dynamic, it always allows full conduction angle, while eliminating the possibility of cross conduction. Because the collector voltage swing of Q1 and Q2 would normally exceed the voltage rating of the AND gates, the resistors and zener diodes are used to clamp the input voltage level to the gates.